Power Quality Improvement of Utility-Distribution System using Self-Supported DSTATCOM based on Unit Template based Control Algorithm in PFC and ZVR Modes

Meenakshi Rastogi¹, Aijaz Ahmad² and Abdul Hamid Bhat³

^{1,2,3}NIT Srinagar, J&K E-mail: ¹meenakshirastogi4@gmail.com, ²aijaz54@nitsri.net, ³bhatdee@nitsri.net

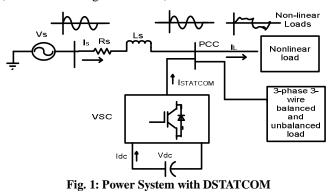
Abstract—Distribution Static Compensator (DSTATCOM) is one of the custom power devices which is used in shunt with the utility distribution system. DSTATCOM protects the distribution systems from various power quality problems like harmonics, load unbalances and other power system issues simultaneously.

In this paper, simplified unit template-based control algorithm is used to extract the reference source current. The generation of reference source current without Phase Locked Loop (PLL)takes more execution time in control algorithm. The standard PLL not only takes more execution time but also increases the reactive power burden on the DSTATCOM. Here, two modes power factor correction (PFC) and zero voltage regulation (ZVR) are used to improve power factor or regulated load voltage.

PFC and ZVR are not possible simultaneously. So, system has been designed separately to achieve one of the objectives(PFC and ZVR) for linear and non-linear loads. MATLAB/SIMULINK model has been designed with3-single phase unbalanced linear and non-linear loads in 3-phase 3-wire system to evaluate the performance of DSTATCOM under unbalanced loading condition and desired results have been obtained. 3-leg 6-pulse Voltage Source Converter (VSC) based self-supported DSTATCOM has been designed. The filter inductance and DC link capacitor have been designed for various linear and non-linear loads. The Total Harmonics Distortion (THD) less than 3% in source voltage and current has been achieved here.

1. INTRODUCTION

Distribution Static Compensator (DSTATCOM) is shunt connected FACTS device which compensates for different power quality problems like harmonics, unbalanced loading, high neutral current and power system issues due to heavy loads like poor power factor and voltage regulation [1-3]. DSTATCOM protects the distribution systems from various power quality problems and other power system issues simultaneously. This is the major advantage of DSTATCOM. So, most of the power quality issue related to the current addresses by the DSTATCOM. The power factor become lagging due to heavy loads like induction motors, which affects the power factor at grid side, so DSTATCOM improves the power factor near to unity at power factor correction mode (PFC) mode. It regulates the load voltage upto nominal value at heavy loading condition at zero voltage Regulation (ZVR) mode. DSTATCOM protects the distribution systems from various power quality problems like harmonics, load unbalances and other power system issues simultaneously. Different nonlinear loads induce harmonics to the point of common coupling (PCC) which reflect to the source side and these harmonics pollute other loads (customers having linear loads).



2. POWER SYSTEM ISSUES AND POWER QUALITY PROBLEMS

2.1 Poor power factor

Due to heavy loading condition, the load current lags more the load voltage, it reflects to the grid side, which results poor power factor at source side [4,5].

2.2 Poor Voltage Regulation

At heavy loading condition, load drags more current, drop will be more so the load voltage is less than nominal value (not equal to the source voltage). So, the voltage regulation will be poor.

2.3 Load Unbalancing

Unbalances in magnitude and phase in three-phase load current occurs due to different single-phase loads. Due to which, the source current become unbalanced [7].

2.4 Harmonics

Due to non-linear loads like single-phase inverters, rectifiers and 3-phase non-linear loads like inverter AC injects harmonics into the system at PCC. These loads infect the other linear loads, PCC current and grid current. So whole system current gets distorted[8].

3. SYSTEM CONFIGURATION AND DSTATCOM DYNAMIC MODEL

3.1 Control of DSTATCOMs in UPF mode of operation

Figure 2 shows the phasor diagram without and with DSTATCOM in PFC mode of operation.

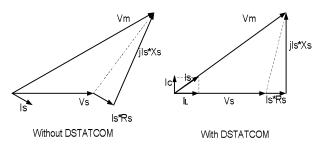


Fig. 2: Phasor diagrams for PFC mode of operation

Fig. 3 shows the unit template-based control algorithm of DSTATCOM for power factor correction (PFC) at PCC. In this control algorithm, three-phase voltage at PCC along with the DC voltage of the DSTATCOM are used for implementing this control algorithm. Three-phase voltage are sensed at PCC and are conditioned in filter to filter out any distortion. For the control of DSTATCOM, the self-supporting DC bus is realised using a PI voltage controller on the DC bus voltage of the DSTATCOM provides the amplitude of in-phase component ($I_{sa}^*, I_{sb}^*, I_{sc}^*$) of the reference current. The three-phase unit current vectors (U_{sa}, U_{sb}, U_{sc}) are derived in-phase with the filtered supply voltage (v_{ma}, v_{mb}, v_{mc}).

The amplitude of reference supply currents is computed using a PI voltage controller over the average value of the DC bus voltage (v_{DCa}) of the DSTATCOM and its reference value (v_{DC}^*).

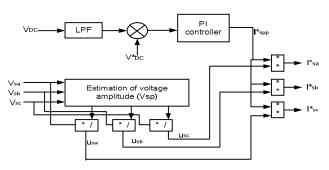


Fig. 3: Unit template-based control algorithm of DSTATCOMs for PFC mode of operation

A comparison of average and reference values of the DC bus voltage of the DSTATCOM results in a voltage error, which is fed to a PI voltage controller.

$$v_{DC}(n) = v_{DC}^{*}(n) - v_{DCa}(n)$$
(1)

This voltage error is fed to a PI voltage controller, and the output of the PI voltage controller is

$$I_{spp}(n) = I_{spp}(n-1) + K_{pd}\{v_{DCe}(n) - v_{DCe}(n-1)\} + K_i dv_{DCe}(n)$$
(2)

Where $v_{DC}(n) = v_{DC}^*(n) - v_{DCa}(n)$ is the error between the reference v_{DC}^* and the sensed (v_{DC}) DC voltage at the nth sampling instant, and K_{pd} and K_{id} are the proportional and integral gain constants of the DC bus voltage PI controller, respectively

Calculation of reference source current

$$I_{sa}^* = I_m * \sin(\omega t) \tag{3}$$

$$I_{sb}^* = I_m * \sin(\omega t - 120) \tag{4}$$

$$I_{sc}^* = I_m * \sin(\omega t + 120) \tag{4}$$

Where I_m = peak of the reference current

Calculation of in-phase unit template

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$$U_{a} = \sin(\omega t) = \frac{V_{a}}{V_{t}}$$
(5)

$$J_{b} = \sin(\omega t - 120) = \frac{V_{b}}{V_{t}}$$
(6)

$$U_{c} = \sin(\omega t + 120) = \frac{V_{c}}{V_{t}}$$
(7)

Calculation of amplitude od source voltage

$$V_t \text{ or } V_{peak} = \left\{ \left(\frac{2}{3}\right) \left(V_{sa}^2 + V_{sb}^2 + V_{sc}^2\right) \right\}^{\frac{1}{2}}$$
(8)

Calculation of in-phase component of reference supply current

$$I_{sad}^* = I_{spp}^* U_{sad} \tag{9}$$

$$I_{sbd}^* = I_{spp}^* U_{sbd} \tag{10}$$

$$I_{scd}^* = I_{spp}^* U_{scd} \tag{11}$$

3.2 Control of DSTATCOMs in ZVR Mode of Operation

The DSTATCOM can compensate the reactive power and negative-sequence currents of the loads. However, because of finite (nonzero) internal impedance of the utility, which is represented by Z_s (L_s , R_s), the voltage waveforms at PCC to other loads are not regulated and result in a voltage drop. The DSTATCOM should regulate the PCC voltages so that other loads connected at PCC are not affected by this voltage drop. The voltage drops are caused by many loads such as inrush currents by the direct-online starting of motors. Thus, it is necessary to switch the operating mode of the DSTATCOM to a voltage regulator.

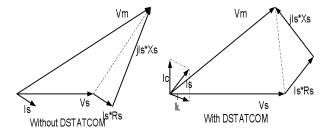


Fig. 4: Phasor diagrams for ZVR mode of operation

As mentioned earlier, in addition to load balancing, the DSTATCOM can also be operated to maintain constant voltage at PCC. For this purpose, the DSTATCOM takes normally a leading current component (in general) due to lagging power factor loads and it is explained using phasor diagrams shown in Figure 4. When the system is operating without a DSTATCOM, the voltage at PCC (V_s) is less than the supply voltage (VM) due to the drop in the supply impedance $Z_s(L_s, R_s)$ as shown in Figure 4. Now with a DSTATCOM connected in the system and drawing a leading current component, the supply current and hence the drop across the supply impedance can be controlled so that the magnitudes of the PCC voltage and supply voltage become equal $(|V_s| = |V_M|)$ as shown in Figure 4 [8]. By controlling the DSTATCOM current, the amplitude and phase of the supply current may be changed to maintain the desired load voltage. Hence, at the same time, both UPF and ZVR functions cannot be achieved. The control algorithm to maintain the desired PCC voltage, the DSTATCOM for ZVR operation at PCC, is shown in Figure 5 [9,10]. Using this algorithm, one can achieve AC voltage regulation at load terminals (at PCC) and load balancing of unbalanced loads. For regulation of voltage at PCC, the three-phase reference supply currents $(i_{sa}^*, i_{sb}^*, i_{sc}^*)$ have two components (direct and quadrature axis, d-q).

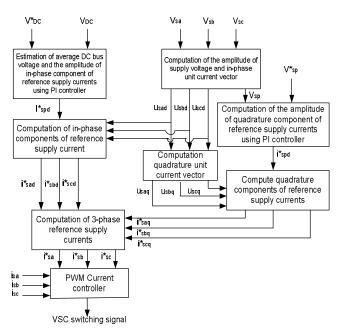


Fig. 5: Unit Template-based control algorithm of DSTATCOMs for ZVR mode of operation

Calculation of quadrature unit template

$$U_{saq} = (-U_{sbd} + U_{scd})/\sqrt{3}$$
 (12)

$$U_{sbq} = (3U_{sad} + U_{sbd} - U_{scd})/2\sqrt{3}$$
(13)

$$U_{scq} = (-3U_{sad} + U_{sbd} - U_{scd})/2\sqrt{3}$$
(14)

Calculation of quadrature component of reference supply current

$$I_{spq}^{*} = I_{smq}(n-1) + K_{pq}\{V_{er}(n) - V_{er}(n-1)\} + K_{iq}\{V_{er}(n)\}$$
(15)

$$I_{saq}^* = I_{spq}^* U_{saq} \tag{16}$$

$$I_{sbq}^* = I_{spq}^* U_{sbq} \tag{17}$$

$$I_{scq}^* = I_{spq}^* U_{scq} \tag{18}$$

Calculation of total reference source current

$$I_{sa}^* = I_{sad}^* + I_{sag}^* \tag{19}$$

$$_{sh}^{*} = I_{shd}^{*} + I_{sha}^{*}$$
(20)

$$I_{sc}^* = I_{scd}^* + I_{scq}^*$$
(21)

4. SIMULATION RESULTS

The DSTATCOM has been connected to the system at 0.2 seconds. Results have been shown before and after the connection od DSTATCOM to evaluate the performance of DSTATCOM First, results have been obtained for PFC mode of operation with linear loads, non-linear loads and unbalanced linear load. Second, results have been obtained for

ZVR mode of operation with the same loads (linear, non-linear and unbalanced linear load).

4.1 Power factor correction for linear loads

The three-phase linear lagging with 0.8 power factor load has been connected to the distribution side. The load active and reactive powers are 8kW and 6kVars respectively. The DC link voltage has been calculated which should be greater than grid voltage. So, the DC link voltage is maintained at 700 V with DSTATCOM shown in figure 6 [11,12].

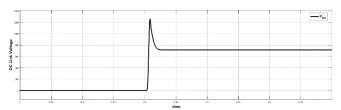


Figure 6. DC Link Voltage

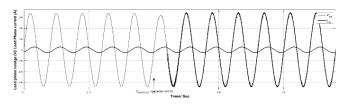


Figure 7. Load Voltage and Current (PFC with linear load

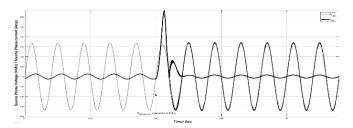


Figure 8. Source Voltage and Current (PFC with linear load

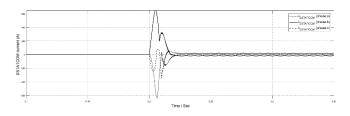


Figure 9. DSTATCOM injected current (PFC with linear load)

4.2. Power factor correction for non-linear loads

The three-phase rectifier load has been connected to the distribution system with 5Ω resistance and 25mH inductance (impedance) at DC side of the three-phase rectifier.

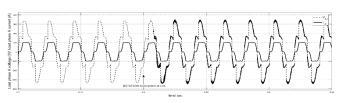


Figure 10: Load voltage and current (PFC with non-linear load)

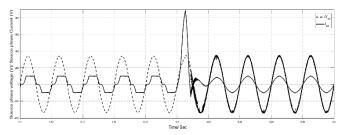


Figure 11. Source Voltage and current (PFC with non-linear load)

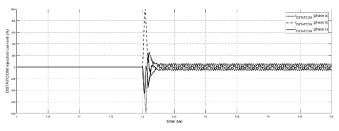


Figure 12: DSTATCOM injected current (PFC with non-linear load)

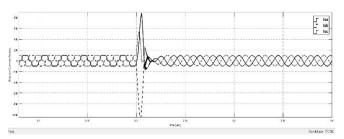


Figure 13: Source current (PFC with linear load)

4.3. Power factor correction for unbalanced linear loads

Three different single-phase with different value of resistances and inductances (different impedances at each phase) have been connected at distribution side to make the load current unbalance.

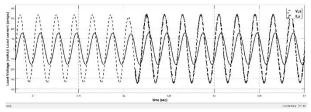


Figure 14: Source Voltage and Current (PFC with unbalanced linear load)

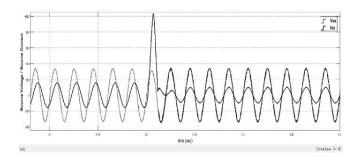


Figure 15. Source Voltage and Current (PFC with unbalanced linear load)

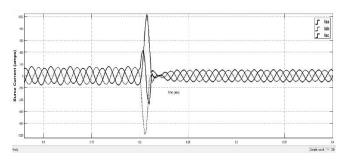


Figure 16. Source current (PFC with unbalanced linear load)

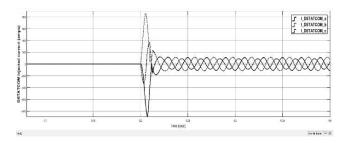


Figure 17. DSTATCOM injected current (PFC with unbalanced linear load)

4.4. Zero Voltage Regulation for linear load

The same loads have been taken for ZVR mode which are used for PFC mode. But load active and reactive power have been increased to make drop at load voltage. The load active and reactive power have been taken as 40kW and 30kVars respectively. Power factor is same as PFC mode of operation.

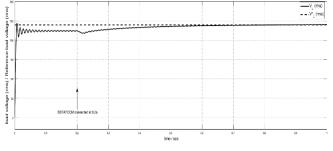


Figure 18. Load Voltage (Reference and Actual)

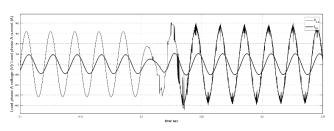


Figure 19. Load Voltage and Current (ZVR with linear load)

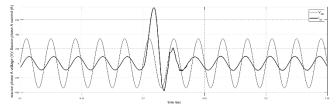


Figure 20. Source Voltage and Current (ZVR with linear load)

4.5. Zero Voltage Regulation for non-linear load

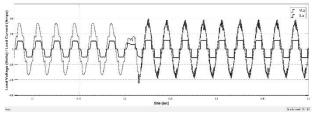


Figure 21. Load voltage and current (ZVR with non-linear load)

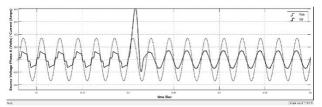


Figure 22. Source Voltage and Current (ZVR with non-linear load)

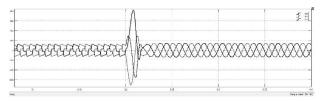
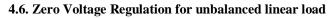
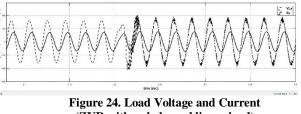


Figure 23. Source Current (ZVR with non-linear load)





(ZVR with unbalanced linear load)

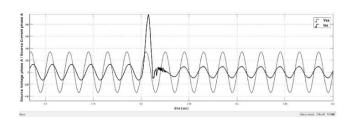


Figure 25. Source Voltage and Current (ZVR with unbalanced linear load)

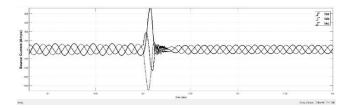


Figure 26. Source Current (ZVR with unbalanced linear load)

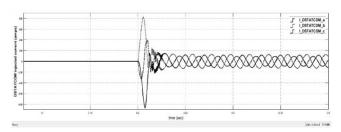


Figure 27. DSTATCOM injected current (ZVR with unbalanced linear load)

Table 1: Total Harmonic Distortion in Source current

Kind of loads		Without DSTATCOM	With DSTATCOM
Non-linear loa	ads	16.61%	2.42%
in PFC mode			
Non-linear loa	ads	21.25 %	2.48%
in ZVR mode			

5. CONCLUSION

The MATLAB/Simulink model based on mathematical equations has been designed, simulated and satisfactory results have been obtained to evaluate the performance of STATCOM at different loads (linear, non-linear and linear unbalanced loads). The two PFC and ZVR modes of operation have been performed. Harmonics in source current have been eliminated due to non-linear loads. The Total Harmonic Distortion (THD) in source current has been achieved less than 3% at different loads which are mentioned in the table I. The filter inductance and DC link capacitance has been designed for the three-phase balanced load. The RC filter has also been designed for the model. So DSTATCOM performs well and solve the power quality related to current, compensates the reactive power required by the power systems, regulates the PCC voltage and improves the power factor of the system.

Table 2: Parameter of the utility distribution system and the local load

Grid Voltage V _m	415 V
Grid Frequencyf _n	50Hz
Grid ResistanceR _s	0.01Ω
Grid InductanceR ₁	.01mH
Load ResistanceL ₁	1.5Ω
Power Factor ϕ	0.8
Feeder Inductance L _{fe}	0.23mH
Ripple Filter RC	5Ω, 6.3µF

Table 3: Parameter of the DSTATCOM system

Coupling transformer inductance L _f	1mH
Coupling Transfer ResistanceR _f	0.01
PI Controller for DC link K _p ,K _i	1, 0.65
PI Controller for PCC voltage K _p , K _i	1, 2
DC Link Voltage V _{DC}	700V
DC link Capacitor C	4700µF
Switching Frequencyf _{sw}	10kHz
Kind of PWM	SPWM

6. ACKNOWLEDGEMENT

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